```
/*****************************************************************************
|*
|*  Module:    regsc509.sfr
|*
|*  Version:   1.3
|*
|*  Copyright 1999-2002 Altium BV
|*
 *****************************************************************************/

#ifndef _REGSC509_SFR
#define _REGSC509_SFR

_sfrbyte P0      _at( 0x80 );
_sfrbyte DIR0        _at( 0x80 );
_sfrbyte SP      _at( 0x81 );
_sfrbyte DPL         _at( 0x82 );
_sfrbyte DPH         _at( 0x83 );
_sfrbyte WDTL        _at( 0x84 );
_sfrbyte WDTH        _at( 0x85 );
_sfrbyte WDTREL      _at( 0x86 );
_sfrbyte PCON        _at( 0x87 );
_sfrbyte TCON        _at( 0x88 );
_sfrbyte TMOD        _at( 0x89 );
_sfrbyte TL0         _at( 0x8A );
_sfrbyte TL1         _at( 0x8B );
_sfrbyte TH0         _at( 0x8C );
_sfrbyte TH1         _at( 0x8D );
_sfrbyte P1      _at( 0x90 );
_sfrbyte DIR1        _at( 0x90 );
_sfrbyte XPAGE       _at( 0x91 );
_sfrbyte DPSEL       _at( 0x92 );
_sfrbyte S0CON       _at( 0x98 );
_sfrbyte S0BUF       _at( 0x99 );
_sfrbyte IEN2        _at( 0x9A );
_sfrbyte S1CON       _at( 0x9B );
_sfrbyte S1BUF       _at( 0x9C );
_sfrbyte S1RELL      _at( 0x9D );
_sfrbyte P2      _at( 0xA0 );
_sfrbyte DIR2        _at( 0xA0 );
_sfrbyte COMSETL     _at( 0xA1 );
_sfrbyte COMSETH     _at( 0xA2 );
_sfrbyte COMCLRL     _at( 0xA3 );
_sfrbyte COMCLRH     _at( 0xA4 );
_sfrbyte SETMSK      _at( 0xA5 );
_sfrbyte CLRMSK      _at( 0xA6 );
_sfrbyte IEN0        _at( 0xA8 );
_sfrbyte IP0         _at( 0xA9 );
_sfrbyte S0RELL      _at( 0xAA );
_sfrbyte P3      _at( 0xB0 );
_sfrbyte DIR3        _at( 0xB0 );
_sfrbyte SYSCON      _at( 0xB1 );
_sfrbyte SYSCON1     _at( 0xB2 );
_sfrbyte FMODE       _at( 0xB3 );
_sfrbyte PRSC        _at( 0xB4 );
_sfrbyte IEN1        _at( 0xB8 );
_sfrbyte IP1         _at( 0xB9 );
_sfrbyte S0RELH      _at( 0xBA );
_sfrbyte S1RELH      _at( 0xBB );
_sfrbyte CT1CON      _at( 0xBC );
_sfrbyte IEN3        _at( 0xBE );
_sfrbyte IRCON2      _at( 0xBF );
_sfrbyte EICC1       _at( 0xBF );
_sfrbyte IRCON0      _at( 0xC0 );
_sfrbyte CCEN        _at( 0xC1 );
_sfrbyte CCL1        _at( 0xC2 );
_sfrbyte CCH1        _at( 0xC3 );
_sfrbyte CCL2        _at( 0xC4 );
_sfrbyte CCH2        _at( 0xC5 );
_sfrbyte CCL3        _at( 0xC6 );
_sfrbyte CCH3        _at( 0xC7 );
_sfrbyte T2CON       _at( 0xC8 );
_sfrbyte CC4EN       _at( 0xC9 );
_sfrbyte CRCL        _at( 0xCA );
_sfrbyte CRCH        _at( 0xCB );
_sfrbyte TL2         _at( 0xCC );
_sfrbyte TH2         _at( 0xCD );
_sfrbyte CCL4        _at( 0xCE );
_sfrbyte CCH4        _at( 0xCF );
_sfrbyte PSW         _at( 0xD0 );
_sfrbyte IRCON1      _at( 0xD1 );
_sfrbyte CML0        _at( 0xD2 );
_sfrbyte CC1L0       _at( 0xD2 );
_sfrbyte CMH0        _at( 0xD3 );
_sfrbyte CC1H0       _at( 0xD3 );
_sfrbyte CML1        _at( 0xD4 );
_sfrbyte CC1L1       _at( 0xD4 );
_sfrbyte CMH1        _at( 0xD5 );
_sfrbyte CC1H1       _at( 0xD5 );
```

```
 90 _sfrbyte CML2        _at( 0xD6 );
    _sfrbyte CC1L2       _at( 0xD6 );
    _sfrbyte CMH2        _at( 0xD7 );
    _sfrbyte CC1H2       _at( 0xD7 );
    _sfrbyte ADCON0      _at( 0xD8 );
 95 _sfrbyte ADDATH      _at( 0xD9 );
    _sfrbyte ADDATL      _at( 0xDA );
    _sfrbyte P7      _at( 0xDB );
    _sfrbyte ADCON1      _at( 0xDC );
    _sfrbyte P8      _at( 0xDD );
100 _sfrbyte CTRELL      _at( 0xDE );
    _sfrbyte CT1RELL     _at( 0xDE );
    _sfrbyte CTRELH      _at( 0xDF );
    _sfrbyte CT1RELH     _at( 0xDF );
    _sfrbyte ACC         _at( 0xE0 );
105 _sfrbyte CTCON       _at( 0xE1 );
    _sfrbyte CML3        _at( 0xE2 );
    _sfrbyte CC1L3       _at( 0xE2 );
    _sfrbyte CMH3        _at( 0xE3 );
    _sfrbyte CC1H3       _at( 0xE3 );
110 _sfrbyte CML4        _at( 0xE4 );
    _sfrbyte CC1L4       _at( 0xE4 );
    _sfrbyte CMH4        _at( 0xE5 );
    _sfrbyte CC1H4       _at( 0xE5 );
    _sfrbyte CML5        _at( 0xE6 );
115 _sfrbyte CC1L5       _at( 0xE6 );
    _sfrbyte CMH5        _at( 0xE7 );
    _sfrbyte CC1H5       _at( 0xE7 );
    _sfrbyte P4      _at( 0xE8 );
    _sfrbyte DIR4        _at( 0xE8 );
120 _sfrbyte MD0         _at( 0xE9 );
    _sfrbyte MD1         _at( 0xEA );
    _sfrbyte MD2         _at( 0xEB );
    _sfrbyte MD3         _at( 0xEC );
    _sfrbyte MD4         _at( 0xED );
125 _sfrbyte MD5         _at( 0xEE );
    _sfrbyte ARCON       _at( 0xEF );
    _sfrbyte B       _at( 0xF0 );
    _sfrbyte CML6        _at( 0xF2 );
    _sfrbyte CC1L6       _at( 0xF2 );
130 _sfrbyte CMH6        _at( 0xF3 );
    _sfrbyte CC1H6       _at( 0xF3 );
    _sfrbyte CML7        _at( 0xF4 );
    _sfrbyte CC1L7       _at( 0xF4 );
    _sfrbyte CMH7        _at( 0xF5 );
135 _sfrbyte CC1H7       _at( 0xF5 );
    _sfrbyte CMEN        _at( 0xF6 );
    _sfrbyte CC1EN       _at( 0xF6 );
    _sfrbyte CMSEL       _at( 0xF7 );
    _sfrbyte CAFR        _at( 0xF7 );
140 _sfrbyte P5      _at( 0xF8 );
    _sfrbyte DIR5        _at( 0xF8 );
    _sfrbyte P9      _at( 0xF9 );
    _sfrbyte DIR9        _at( 0xF9 );
    _sfrbyte P6      _at( 0xFA );
145 _sfrbyte DIR6        _at( 0xFA );

    /* defining bits in SFR DIR0 */
    _sfrbit P0_0     _atbit( DIR0, 0 );
    _sfrbit P0_1     _atbit( DIR0, 1 );
150 _sfrbit P0_2     _atbit( DIR0, 2 );
    _sfrbit P0_3     _atbit( DIR0, 3 );
    _sfrbit P0_4     _atbit( DIR0, 4 );
    _sfrbit P0_5     _atbit( DIR0, 5 );
    _sfrbit P0_6     _atbit( DIR0, 6 );
155 _sfrbit P0_7     _atbit( DIR0, 7 );

    #define bmP0_0  0x01
    #define bmP0_1  0x02
    #define bmP0_2  0x04
160 #define bmP0_3  0x08
    #define bmP0_4  0x10
    #define bmP0_5  0x20
    #define bmP0_6  0x40
    #define bmP0_7  0x80
165
    #define SET_P0_0    P0_0 = 1;
    #define CLR_P0_0    P0_0 = 0;
    #define GET_P0_0    P0_0
    #define SET_P0_1    P0_1 = 1;
170 #define CLR_P0_1    P0_1 = 0;
    #define GET_P0_1    P0_1
    #define SET_P0_2    P0_2 = 1;
    #define CLR_P0_2    P0_2 = 0;
    #define GET_P0_2    P0_2
175 #define SET_P0_3    P0_3 = 1;
    #define CLR_P0_3    P0_3 = 0;
    #define GET_P0_3    P0_3
    #define SET_P0_4    P0_4 = 1;
```

```
#define ompiling error_1.c
|*
|*  Copyright 1999-2002 Altium BV
|*
 ************************************************************************/

#ifndef _REGSC509_SFR
#define _REGSC509_SFR

_sfrbyte P0     _at( 0x80 );
_sfrbyte DIR0       _at( 0x80 );
_sfrbyte SP     _at( 0x81 );
_sfrbyte DPL        _at( 0x82 );
_sfrbyte DPH        _at( 0x83 );
_sfrbyte WDTL       _at( 0x84 );
_sfrbyte WDTH       _at( 0x85 );
_sfrbyte WDTREL     _at( 0x86 );
_sfrbyte PCON       _at( 0x87 );
_sfrbyte TCON       _at( 0x88 );
_sfrbyte TMOD       _at( 0x89 );
_sfrbyte TL0        _at( 0x8A );
_sfrbyte TL1        _at( 0x8B );
_sfrbyte TH0        _at( 0x8C );
_sfrbyte TH1        _at( 0x8D );
_sfrbyte P1     _at( 0x90 );
_sfrbyte DIR1       _at( 0x90 );
_sfrbyte XPAGE      _at( 0x91 );
_sfrbyte DPSEL      _at( 0x92 );
_sfrbyte S0CON      _at( 0x98 );
_sfrbyte S0BUF      _at( 0x99 );
_sfrbyte IEN2       _at( 0x9A );
_sfrbyte S1CON      _at( 0x9B );
_sfrbyte S1BUF      _at( 0x9C );
_sfrbyte S1RELL     _at( 0x9D );
_sfrbyte P2     _at( 0xA0 );
_sfrbyte DIR2       _at( 0xA0 );
_sfrbyte COMSETL    _at( 0xA1 );
_sfrbyte COMSETH    _at( 0xA2 );
_sfrbyte COMCLRL    _at( 0xA3 );
_sfrbyte COMCLRH    _at( 0xA4 );
_sfrbyte SETMSK     _at( 0xA5 );
_sfrbyte CLRMSK     _at( 0xA6 );
_sfrbyte IEN0       _at( 0xA8 );
_sfrbyte IP0        _at( 0xA9 );
_sfrbyte S0RELL     _at( 0xAA );
_sfrbyte P3     _at( 0xB0 );
_sfrbyte DIR3       _at( 0xB0 );
_sfrbyte SYSCON     _at( 0xB1 );
_sfrbyte SYSCON1    _at( 0xB2 );
_sfrbyte FMODE      _at( 0xB3 );
_sfrbyte PRSC       _at( 0xB4 );
_sfrbyte IEN1       _at( 0xB8 );
_sfrbyte IP1        _at( 0xB9 );
_sfrbyte S0RELH     _at( 0xBA );
_sfrbyte S1RELH     _at( 0xBB );
_sfrbyte CT1CON     _at( 0xBC );
_sfrbyte IEN3       _at( 0xBE );
_sfrbyte IRCON2     _at( 0xBF );
_sfrbyte EICC1      _at( 0xBF );
_sfrbyte IRCON0     _at( 0xC0 );
_sfrbyte CCEN       _at( 0xC1 );
_sfrbyte CCL1       _at( 0xC2 );
_sfrbyte CCH1       _at( 0xC3 );
_sfrbyte CCL2       _at( 0xC4 );
_sfrbyte CCH2       _at( 0xC5 );
_sfrbyte CCL3       _at( 0xC6 );
_sfrbyte CCH3       _at( 0xC7 );
_sfrbyte T2CON      _at( 0xC8 );
_sfrbyte CC4EN      _at( 0xC9 );
_sfrbyte CRCL       _at( 0xCA );
_sfrbyte CRCH       _at( 0xCB );
_sfrbyte TL2        _at( 0xCC );
_sfrbyte TH2        _at( 0xCD );
_sfrbyte CCL4       _at( 0xCE );
_sfrbyte CCH4       _at( 0xCF );
_sfrbyte PSW        _at( 0xD0 );
_sfrbyte IRCON1     _at( 0xD1 );
_sfrbyte CML0       _at( 0xD2 );
_sfrbyte CC1L0      _at( 0xD2 );
_sfrbyte CMH0       _at( 0xD3 );
_sfrbyte CC1H0      _at( 0xD3 );
_sfrbyte CML1       _at( 0xD4 );
_sfrbyte CC1L1      _at( 0xD4 );
_sfrbyte CMH1       _at( 0xD5 );
_sfrbyte CC1H1      _at( 0xD5 );
_sfrbyte CML2       _at( 0xD6 );
_sfrbyte CC1L2      _at( 0xD6 );
_sfrbyte CMH2       _at( 0xD7 );
_sfrbyte CC1H2      _at( 0xD7 );
```

```
    _sfrbyte ADCON0     _at( 0xD8 );
 95 _sfrbyte ADDATH     _at( 0xD9 );
    _sfrbyte ADDATL     _at( 0xDA );
    _sfrbyte P7      _at( 0xDB );
    _sfrbyte ADCON1     _at( 0xDC );
    _sfrbyte P8      _at( 0xDD );
100 _sfrbyte CTRELL     _at( 0xDE );
    _sfrbyte CT1RELL    _at( 0xDE );
    _sfrbyte CTRELH     _at( 0xDF );
    _sfrbyte CT1RELH    _at( 0xDF );
    _sfrbyte ACC        _at( 0xE0 );
105 _sfrbyte CTCON      _at( 0xE1 );
    _sfrbyte CML3       _at( 0xE2 );
    _sfrbyte CC1L3      _at( 0xE2 );
    _sfrbyte CMH3       _at( 0xE3 );
    _sfrbyte CC1H3      _at( 0xE3 );
110 _sfrbyte CML4       _at( 0xE4 );
    _sfrbyte CC1L4      _at( 0xE4 );
    _sfrbyte CMH4       _at( 0xE5 );
    _sfrbyte CC1H4      _at( 0xE5 );
    _sfrbyte CML5       _at( 0xE6 );
115 _sfrbyte CC1L5      _at( 0xE6 );
    _sfrbyte CMH5       _at( 0xE7 );
    _sfrbyte CC1H5      _at( 0xE7 );
    _sfrbyte P4      _at( 0xE8 );
    _sfrbyte DIR4       _at( 0xE8 );
120 _sfrbyte MD0        _at( 0xE9 );
    _sfrbyte MD1        _at( 0xEA );
    _sfrbyte MD2        _at( 0xEB );
    _sfrbyte MD3        _at( 0xEC );
    _sfrbyte MD4        _at( 0xED );
125 _sfrbyte MD5        _at( 0xEE );
    _sfrbyte ARCON      _at( 0xEF );
    _sfrbyte B       _at( 0xF0 );
    _sfrbyte CML6       _at( 0xF2 );
    _sfrbyte CC1L6      _at( 0xF2 );
130 _sfrbyte CMH6       _at( 0xF3 );
    _sfrbyte CC1H6      _at( 0xF3 );
    _sfrbyte CML7       _at( 0xF4 );
    _sfrbyte CC1L7      _at( 0xF4 );
    _sfrbyte CMH7       _at( 0xF5 );
135 _sfrbyte CC1H7      _at( 0xF5 );
    _sfrbyte CMEN       _at( 0xF6 );
    _sfrbyte CC1EN      _at( 0xF6 );
    _sfrbyte CMSEL      _at( 0xF7 );
    _sfrbyte CAFR       _at( 0xF7 );
140 _sfrbyte P5      _at( 0xF8 );
    _sfrbyte DIR5       _at( 0xF8 );
    _sfrbyte P9      _at( 0xF9 );
    _sfrbyte DIR9       _at( 0xF9 );
    _sfrbyte P6      _at( 0xFA );
145 _sfrbyte DIR6       _at( 0xFA );

    /* defining bits in SFR DIR0 */
    _sfrbit P0_0    _atbit( DIR0, 0 );
    _sfrbit P0_1    _atbit( DIR0, 1 );
150 _sfrbit P0_2    _atbit( DIR0, 2 );
    _sfrbit P0_3    _atbit( DIR0, 3 );
    _sfrbit P0_4    _atbit( DIR0, 4 );
    _sfrbit P0_5    _atbit( DIR0, 5 );
    _sfrbit P0_6    _atbit( DIR0, 6 );
155 _sfrbit P0_7    _atbit( DIR0, 7 );

    #define bmP0_0  0x01
    #define bmP0_1  0x02
    #define bmP0_2  0x04
160 #define bmP0_3  0x08
    #define bmP0_4  0x10
    #define bmP0_5  0x20
    #define bmP0_6  0x40
    #define bmP0_7  0x80
165
    #define SET_P0_0    P0_0 = 1;
    #define CLR_P0_0    P0_0 = 0;
    #define GET_P0_0    P0_0
    #define SET_P0_1    P0_1 = 1;
170 #define CLR_P0_1    P0_1 = 0;
    #define GET_P0_1    P0_1
    #define SET_P0_2    P0_2 = 1;
    #define CLR_P0_2    P0_2 = 0;
    #define GET_P0_2    P0_2
175 #define SET_P0_3    P0_3 = 1;
    #define CLR_P0_3    P0_3 = 0;
    #define GET_P0_3    P0_3
    #define SET_P0_4    P0_4 = 1;
    #define CLR_P0_4    P0_4 = 0;
180 #define GET_P0_4    P0_4
    #define SET_P0_5    P0_5 = 1;
    #define CLR_P0_5    P0_5 = 0;
```

```
#define GET_P0_5    P0_5
#define SET_P0_6    P0_6 = 1;
#define CLR_P0_6    P0_6 = 0;
#define GET_P0_6    P0_6
#define SET_P0_7    P0_7 = 1;
#define CLR_P0_7    P0_7 = 0;
#define GET_P0_7    P0_7

/* defining bits in SFR TCON */
_sfrbit IT0 _atbit( TCON, 0 );
_sfrbit IE0 _atbit( TCON, 1 );
_sfrbit IT1 _atbit( TCON, 2 );
_sfrbit IE1 _atbit( TCON, 3 );
_sfrbit TR0 _atbit( TCON, 4 );
_sfrbit TF0 _atbit( TCON, 5 );
_sfrbit TR1 _atbit( TCON, 6 );
_sfrbit TF1 _atbit( TCON, 7 );

#define bmIT0   0x01
#define bmIE0   0x02
#define bmIT1   0x04
#define bmIE1   0x08
#define bmTR0   0x10
#define bmTF0   0x20
#define bmTR1   0x40
#define bmTF1   0x80

#define SET_IT0 IT0 = 1;
#define CLR_IT0 IT0 = 0;
#define GET_IT0 IT0
#define SET_IE0 IE0 = 1;
#define CLR_IE0 IE0 = 0;
#define GET_IE0 IE0
#define SET_IT1 IT1 = 1;
#define CLR_IT1 IT1 = 0;
#define GET_IT1 IT1
#define SET_IE1 IE1 = 1;
#define CLR_IE1 IE1 = 0;
#define GET_IE1 IE1
#define SET_TR0 TR0 = 1;
#define CLR_TR0 TR0 = 0;
#define GET_TR0 TR0
#define SET_TF0 TF0 = 1;
#define CLR_TF0 TF0 = 0;
#define GET_TF0 TF0
#define SET_TR1 TR1 = 1;
#define CLR_TR1 TR1 = 0;
#define GET_TR1 TR1
#define SET_TF1 TF1 = 1;
#define CLR_TF1 TF1 = 0;
#define GET_TF1 TF1

/* defining bits in SFR DIR1 */
_sfrbit CC0 _atbit( DIR1, 0 );
_sfrbit INT3    _atbit( DIR1, 0 );
_sfrbit P1_0    _atbit( DIR1, 0 );
_sfrbit CC1 _atbit( DIR1, 1 );
_sfrbit INT4    _atbit( DIR1, 1 );
_sfrbit P1_1    _atbit( DIR1, 1 );
_sfrbit CC2 _atbit( DIR1, 2 );
_sfrbit INT5    _atbit( DIR1, 2 );
_sfrbit P1_2    _atbit( DIR1, 2 );
_sfrbit CC3 _atbit( DIR1, 3 );
_sfrbit INT6    _atbit( DIR1, 3 );
_sfrbit P1_3    _atbit( DIR1, 3 );
_sfrbit CC4 _atbit( DIR1, 4 );
_sfrbit INT2    _atbit( DIR1, 4 );
_sfrbit P1_4    _atbit( DIR1, 4 );
_sfrbit P1_5    _atbit( DIR1, 5 );
_sfrbit T2EX    _atbit( DIR1, 5 );
_sfrbit CLKOUT  _atbit( DIR1, 6 );
_sfrbit P1_6    _atbit( DIR1, 6 );
_sfrbit P1_7    _atbit( DIR1, 7 );
_sfrbit T2  _atbit( DIR1, 7 );

#define bmCC0   0x01
#define bmINT3  0x01
#define bmP1_0  0x01
#define bmCC1   0x02
#define bmINT4  0x02
#define bmP1_1  0x02
#define bmCC2   0x04
#define bmINT5  0x04
#define bmP1_2  0x04
#define bmCC3   0x08
#define bmINT6  0x08
#define bmP1_3  0x08
#define bmCC4   0x10
#define bmINT2  0x10
```

```
#define bmP1_4  0x10
#define bmP1_5  0x20
#define bmT2EX  0x20
#define bmCLKOUT    0x40
#define bmP1_6  0x40
#define bmP1_7  0x80
#define bmT2    0x80

#define SET_CC0 CC0 = 1;
#define CLR_CC0 CC0 = 0;
#define GET_CC0 CC0
#define SET_INT3    INT3 = 1;
#define CLR_INT3    INT3 = 0;
#define GET_INT3    INT3
#define SET_P1_0    P1_0 = 1;
#define CLR_P1_0    P1_0 = 0;
#define GET_P1_0    P1_0
#define SET_CC1 CC1 = 1;
#define CLR_CC1 CC1 = 0;
#define GET_CC1 CC1
#define SET_INT4    INT4 = 1;
#define CLR_INT4    INT4 = 0;
#define GET_INT4    INT4
#define SET_P1_1    P1_1 = 1;
#define CLR_P1_1    P1_1 = 0;
#define GET_P1_1    P1_1
#define SET_CC2 CC2 = 1;
#define CLR_CC2 CC2 = 0;
#define GET_CC2 CC2
#define SET_INT5    INT5 = 1;
#define CLR_INT5    INT5 = 0;
#define GET_INT5    INT5
#define SET_P1_2    P1_2 = 1;
#define CLR_P1_2    P1_2 = 0;
#define GET_P1_2    P1_2
#define SET_CC3 CC3 = 1;
#define CLR_CC3 CC3 = 0;
#define GET_CC3 CC3
#define SET_INT6    INT6 = 1;
#define CLR_INT6    INT6 = 0;
#define GET_INT6    INT6
#define SET_P1_3    P1_3 = 1;
#define CLR_P1_3    P1_3 = 0;
#define GET_P1_3    P1_3
#define SET_CC4 CC4 = 1;
#define CLR_CC4 CC4 = 0;
#define GET_CC4 CC4
#define SET_INT2    INT2 = 1;
#define CLR_INT2    INT2 = 0;
#define GET_INT2    INT2
#define SET_P1_4    P1_4 = 1;
#define CLR_P1_4    P1_4 = 0;
#define GET_P1_4    P1_4
#define SET_P1_5    P1_5 = 1;
#define CLR_P1_5    P1_5 = 0;
#define GET_P1_5    P1_5
#define SET_T2EX    T2EX = 1;
#define CLR_T2EX    T2EX = 0;
#define GET_T2EX    T2EX
#define SET_CLKOUT  CLKOUT = 1;
#define CLR_CLKOUT  CLKOUT = 0;
#define GET_CLKOUT  CLKOUT
#define SET_P1_6    P1_6 = 1;
#define CLR_P1_6    P1_6 = 0;
#define GET_P1_6    P1_6
#define SET_P1_7    P1_7 = 1;
#define CLR_P1_7    P1_7 = 0;
#define GET_P1_7    P1_7
#define SET_T2  T2 = 1;
#define CLR_T2  T2 = 0;
#define GET_T2  T2

/* defining bits in SFR S0CON */
_sfrbit RI0 _atbit( S0CON, 0 );
_sfrbit TI0 _atbit( S0CON, 1 );
_sfrbit RB80    _atbit( S0CON, 2 );
_sfrbit TB80    _atbit( S0CON, 3 );
_sfrbit REN0    _atbit( S0CON, 4 );
_sfrbit SM20    _atbit( S0CON, 5 );
_sfrbit SM1 _atbit( S0CON, 6 );
_sfrbit SM0 _atbit( S0CON, 7 );

#define bmRI0   0x01
#define bmTI0   0x02
#define bmRB80  0x04
#define bmTB80  0x08
#define bmREN0  0x10
#define bmSM20  0x20
#define bmSM1   0x40
```

```
    #define bmSM0   0x80

    #define SET_RI0 RI0 = 1;
    #define CLR_RI0 RI0 = 0;
365 #define GET_RI0 RI0
    #define SET_TI0 TI0 = 1;
    #define CLR_TI0 TI0 = 0;
    #define GET_TI0 TI0
    #define SET_RB80    RB80 = 1;
370 #define CLR_RB80    RB80 = 0;
    #define GET_RB80    RB80
    #define SET_TB80    TB80 = 1;
    #define CLR_TB80    TB80 = 0;
    #define GET_TB80    TB80
375 #define SET_REN0    REN0 = 1;
    #define CLR_REN0    REN0 = 0;
    #define GET_REN0    REN0
    #define SET_SM20    SM20 = 1;
    #define CLR_SM20    SM20 = 0;
380 #define GET_SM20    SM20
    #define SET_SM1 SM1 = 1;
    #define CLR_SM1 SM1 = 0;
    #define GET_SM1 SM1
    #define SET_SM0 SM0 = 1;
385 #define CLR_SM0 SM0 = 0;
    #define GET_SM0 SM0

    /* defining bits in SFR DIR2 */
    _sfrbit P2_0    _atbit( DIR2, 0 );
390 _sfrbit P2_1    _atbit( DIR2, 1 );
    _sfrbit P2_2    _atbit( DIR2, 2 );
    _sfrbit P2_3    _atbit( DIR2, 3 );
    _sfrbit P2_4    _atbit( DIR2, 4 );
    _sfrbit P2_5    _atbit( DIR2, 5 );
395 _sfrbit P2_6    _atbit( DIR2, 6 );
    _sfrbit P2_7    _atbit( DIR2, 7 );

    #define bmP2_0  0x01
    #define bmP2_1  0x02
400 #define bmP2_2  0x04
    #define bmP2_3  0x08
    #define bmP2_4  0x10
    #define bmP2_5  0x20
    #define bmP2_6  0x40
405 #define bmP2_7  0x80

    #define SET_P2_0    P2_0 = 1;
    #define CLR_P2_0    P2_0 = 0;
    #define GET_P2_0    P2_0
410 #define SET_P2_1    P2_1 = 1;
    #define CLR_P2_1    P2_1 = 0;
    #define GET_P2_1    P2_1
    #define SET_P2_2    P2_2 = 1;
    #define CLR_P2_2    P2_2 = 0;
415 #define GET_P2_2    P2_2
    #define SET_P2_3    P2_3 = 1;
    #define CLR_P2_3    P2_3 = 0;
    #define GET_P2_3    P2_3
    #define SET_P2_4    P2_4 = 1;
420 #define CLR_P2_4    P2_4 = 0;
    #define GET_P2_4    P2_4
    #define SET_P2_5    P2_5 = 1;
    #define CLR_P2_5    P2_5 = 0;
    #define GET_P2_5    P2_5
425 #define SET_P2_6    P2_6 = 1;
    #define CLR_P2_6    P2_6 = 0;
    #define GET_P2_6    P2_6
    #define SET_P2_7    P2_7 = 1;
    #define CLR_P2_7    P2_7 = 0;
430 #define GET_P2_7    P2_7

    /* defining bits in SFR IEN0 */
    _sfrbit EX0 _atbit( IEN0, 0 );
    _sfrbit ET0 _atbit( IEN0, 1 );
435 _sfrbit EX1 _atbit( IEN0, 2 );
    _sfrbit ET1 _atbit( IEN0, 3 );
    _sfrbit ES0 _atbit( IEN0, 4 );
    _sfrbit ET2 _atbit( IEN0, 5 );
    _sfrbit WDT _atbit( IEN0, 6 );
440 _sfrbit EAL _atbit( IEN0, 7 );

    #define bmEX0   0x01
    #define bmET0   0x02
    #define bmEX1   0x04
445 #define bmET1   0x08
    #define bmES0   0x10
    #define bmET2   0x20
    #define bmWDT   0x40
    #define bmEAL   0x80
```

```
450
    #define SET_EX0 EX0 = 1;
    #define CLR_EX0 EX0 = 0;
    #define GET_EX0 EX0
    #define SET_ET0 ET0 = 1;
455 #define CLR_ET0 ET0 = 0;
    #define GET_ET0 ET0
    #define SET_EX1 EX1 = 1;
    #define CLR_EX1 EX1 = 0;
    #define GET_EX1 EX1
460 #define SET_ET1 ET1 = 1;
    #define CLR_ET1 ET1 = 0;
    #define GET_ET1 ET1
    #define SET_ES0 ES0 = 1;
    #define CLR_ES0 ES0 = 0;
465 #define GET_ES0 ES0
    #define SET_ET2 ET2 = 1;
    #define CLR_ET2 ET2 = 0;
    #define GET_ET2 ET2
    #define SET_WDT WDT = 1;
470 #define CLR_WDT WDT = 0;
    #define GET_WDT WDT
    #define SET_EAL EAL = 1;
    #define CLR_EAL EAL = 0;
    #define GET_EAL EAL
475
    /* defining bits in SFR DIR3 */
    _sfrbit P3_0    _atbit( DIR3, 0 );
    _sfrbit RXD _atbit( DIR3, 0 );
    _sfrbit P3_1    _atbit( DIR3, 1 );
480 _sfrbit TXD _atbit( DIR3, 1 );
    _sfrbit INT0    _atbit( DIR3, 2 );
    _sfrbit P3_2    _atbit( DIR3, 2 );
    _sfrbit INT1    _atbit( DIR3, 3 );
    _sfrbit P3_3    _atbit( DIR3, 3 );
485 _sfrbit P3_4    _atbit( DIR3, 4 );
    _sfrbit T0  _atbit( DIR3, 4 );
    _sfrbit P3_5    _atbit( DIR3, 5 );
    _sfrbit T1  _atbit( DIR3, 5 );
    _sfrbit P3_6    _atbit( DIR3, 6 );
490 _sfrbit WR  _atbit( DIR3, 6 );
    _sfrbit P3_7    _atbit( DIR3, 7 );
    _sfrbit RD  _atbit( DIR3, 7 );

    #define bmP3_0  0x01
495 #define bmRXD   0x01
    #define bmP3_1  0x02
    #define bmTXD   0x02
    #define bmINT0  0x04
    #define bmP3_2  0x04
500 #define bmINT1  0x08
    #define bmP3_3  0x08
    #define bmP3_4  0x10
    #define bmT0    0x10
    #define bmP3_5  0x20
505 #define bmT1    0x20
    #define bmP3_6  0x40
    #define bmWR    0x40
    #define bmP3_7  0x80
    #define bmRD    0x80
510
    #define SET_P3_0    P3_0 = 1;
    #define CLR_P3_0    P3_0 = 0;
    #define GET_P3_0    P3_0
    #define SET_RXD RXD = 1;
515 #define CLR_RXD RXD = 0;
    #define GET_RXD RXD
    #define SET_P3_1    P3_1 = 1;
    #define CLR_P3_1    P3_1 = 0;
    #define GET_P3_1    P3_1
520 #define SET_TXD TXD = 1;
    #define CLR_TXD TXD = 0;
    #define GET_TXD TXD
    #define SET_INT0    INT0 = 1;
    #define CLR_INT0    INT0 = 0;
525 #define GET_INT0    INT0
    #define SET_P3_2    P3_2 = 1;
    #define CLR_P3_2    P3_2 = 0;
    #define GET_P3_2    P3_2
    #define SET_INT1    INT1 = 1;
530 #define CLR_INT1    INT1 = 0;
    #define GET_INT1    INT1
    #define SET_P3_3    P3_3 = 1;
    #define CLR_P3_3    P3_3 = 0;
    #define GET_P3_3    P3_3
535 #define SET_P3_4    P3_4 = 1;
    #define CLR_P3_4    P3_4 = 0;
    #define GET_P3_4    P3_4
    #define SET_T0  T0 = 1;
```

```
#define CLR_T0  T0 = 0;
#define GET_T0  T0
#define SET_P3_5    P3_5 = 1;
#define CLR_P3_5    P3_5 = 0;
#define GET_P3_5    P3_5
#define SET_T1  T1 = 1;
#define CLR_T1  T1 = 0;
#define GET_T1  T1
#define SET_P3_6    P3_6 = 1;
#define CLR_P3_6    P3_6 = 0;
#define GET_P3_6    P3_6
#define SET_WR  WR = 1;
#define CLR_WR  WR = 0;
#define GET_WR  WR
#define SET_P3_7    P3_7 = 1;
#define CLR_P3_7    P3_7 = 0;
#define GET_P3_7    P3_7
#define SET_RD  RD = 1;
#define CLR_RD  RD = 0;
#define GET_RD  RD

/* defining bits in SFR IEN1 */
_sfrbit EADC    _atbit( IEN1, 0 );
_sfrbit EX2 _atbit( IEN1, 1 );
_sfrbit EX3 _atbit( IEN1, 2 );
_sfrbit EX4 _atbit( IEN1, 3 );
_sfrbit EX5 _atbit( IEN1, 4 );
_sfrbit EX6 _atbit( IEN1, 5 );
_sfrbit SWDT    _atbit( IEN1, 6 );
_sfrbit EXEN2   _atbit( IEN1, 7 );

#define bmEADC  0x01
#define bmEX2   0x02
#define bmEX3   0x04
#define bmEX4   0x08
#define bmEX5   0x10
#define bmEX6   0x20
#define bmSWDT  0x40
#define bmEXEN2 0x80

#define SET_EADC    EADC = 1;
#define CLR_EADC    EADC = 0;
#define GET_EADC    EADC
#define SET_EX2 EX2 = 1;
#define CLR_EX2 EX2 = 0;
#define GET_EX2 EX2
#define SET_EX3 EX3 = 1;
#define CLR_EX3 EX3 = 0;
#define GET_EX3 EX3
#define SET_EX4 EX4 = 1;
#define CLR_EX4 EX4 = 0;
#define GET_EX4 EX4
#define SET_EX5 EX5 = 1;
#define CLR_EX5 EX5 = 0;
#define GET_EX5 EX5
#define SET_EX6 EX6 = 1;
#define CLR_EX6 EX6 = 0;
#define GET_EX6 EX6
#define SET_SWDT    SWDT = 1;
#define CLR_SWDT    SWDT = 0;
#define GET_SWDT    SWDT
#define SET_EXEN2   EXEN2 = 1;
#define CLR_EXEN2   EXEN2 = 0;
#define GET_EXEN2   EXEN2

/* defining bits in SFR IRCON0 */
_sfrbit IADC    _atbit( IRCON0, 0 );
_sfrbit IEX2    _atbit( IRCON0, 1 );
_sfrbit IEX3    _atbit( IRCON0, 2 );
_sfrbit IEX4    _atbit( IRCON0, 3 );
_sfrbit IEX5    _atbit( IRCON0, 4 );
_sfrbit IEX6    _atbit( IRCON0, 5 );
_sfrbit TF2 _atbit( IRCON0, 6 );
_sfrbit EXF2    _atbit( IRCON0, 7 );

#define bmIADC  0x01
#define bmIEX2  0x02
#define bmIEX3  0x04
#define bmIEX4  0x08
#define bmIEX5  0x10
#define bmIEX6  0x20
#define bmTF2   0x40
#define bmEXF2  0x80

#define SET_IADC    IADC = 1;
#define CLR_IADC    IADC = 0;
#define GET_IADC    IADC
#define SET_IEX2    IEX2 = 1;
#define CLR_IEX2    IEX2 = 0;
```

```
#define GET_IEX2    IEX2
#define SET_IEX3    IEX3 = 1;
#define CLR_IEX3    IEX3 = 0;
#define GET_IEX3    IEX3
#define SET_IEX4    IEX4 = 1;
#define CLR_IEX4    IEX4 = 0;
#define GET_IEX4    IEX4
#define SET_IEX5    IEX5 = 1;
#define CLR_IEX5    IEX5 = 0;
#define GET_IEX5    IEX5
#define SET_IEX6    IEX6 = 1;
#define CLR_IEX6    IEX6 = 0;
#define GET_IEX6    IEX6
#define SET_TF2 TF2 = 1;
#define CLR_TF2 TF2 = 0;
#define GET_TF2 TF2
#define SET_EXF2    EXF2 = 1;
#define CLR_EXF2    EXF2 = 0;
#define GET_EXF2    EXF2

/* defining bits in SFR T2CON */
_sfrbit T2I0    _atbit( T2CON, 0 );
_sfrbit T2I1    _atbit( T2CON, 1 );
_sfrbit T2CM    _atbit( T2CON, 2 );
_sfrbit T2R0    _atbit( T2CON, 3 );
_sfrbit T2R1    _atbit( T2CON, 4 );
_sfrbit I2FR    _atbit( T2CON, 5 );
_sfrbit I3FR    _atbit( T2CON, 6 );
_sfrbit T2PS    _atbit( T2CON, 7 );

#define bmT2I0  0x01
#define bmT2I1  0x02
#define bmT2CM  0x04
#define bmT2R0  0x08
#define bmT2R1  0x10
#define bmI2FR  0x20
#define bmI3FR  0x40
#define bmT2PS  0x80

#define SET_T2I0    T2I0 = 1;
#define CLR_T2I0    T2I0 = 0;
#define GET_T2I0    T2I0
#define SET_T2I1    T2I1 = 1;
#define CLR_T2I1    T2I1 = 0;
#define GET_T2I1    T2I1
#define SET_T2CM    T2CM = 1;
#define CLR_T2CM    T2CM = 0;
#define GET_T2CM    T2CM
#define SET_T2R0    T2R0 = 1;
#define CLR_T2R0    T2R0 = 0;
#define GET_T2R0    T2R0
#define SET_T2R1    T2R1 = 1;
#define CLR_T2R1    T2R1 = 0;
#define GET_T2R1    T2R1
#define SET_I2FR    I2FR = 1;
#define CLR_I2FR    I2FR = 0;
#define GET_I2FR    I2FR
#define SET_I3FR    I3FR = 1;
#define CLR_I3FR    I3FR = 0;
#define GET_I3FR    I3FR
#define SET_T2PS    T2PS = 1;
#define CLR_T2PS    T2PS = 0;
#define GET_T2PS    T2PS

/* defining bits in SFR PSW */
_sfrbit P   _atbit( PSW, 0 );
_sfrbit F1  _atbit( PSW, 1 );
_sfrbit OV  _atbit( PSW, 2 );
_sfrbit RS0 _atbit( PSW, 3 );
_sfrbit RS1 _atbit( PSW, 4 );
_sfrbit F0  _atbit( PSW, 5 );
_sfrbit AC  _atbit( PSW, 6 );
_sfrbit CY  _atbit( PSW, 7 );

#define bmP 0x01
#define bmF1    0x02
#define bmOV    0x04
#define bmRS0   0x08
#define bmRS1   0x10
#define bmF0    0x20
#define bmAC    0x40
#define bmCY    0x80

#define SET_P   P = 1;
#define CLR_P   P = 0;
#define GET_P   P
#define SET_F1  F1 = 1;
#define CLR_F1  F1 = 0;
#define GET_F1  F1
```

```
#define SET_OV  OV = 1;
#define CLR_OV  OV = 0;
#define GET_OV  OV
#define SET_RS0 RS0 = 1;
#define CLR_RS0 RS0 = 0;
#define GET_RS0 RS0
#define SET_RS1 RS1 = 1;
#define CLR_RS1 RS1 = 0;
#define GET_RS1 RS1
#define SET_F0  F0 = 1;
#define CLR_F0  F0 = 0;
#define GET_F0  F0
#define SET_AC  AC = 1;
#define CLR_AC  AC = 0;
#define GET_AC  AC
#define SET_CY  CY = 1;
#define CLR_CY  CY = 0;
#define GET_CY  CY

/* defining bits in SFR ADCON0 */
_sfrbit MX0 _atbit( ADCON0, 0 );
_sfrbit MX1 _atbit( ADCON0, 1 );
_sfrbit MX2 _atbit( ADCON0, 2 );
_sfrbit ADM _atbit( ADCON0, 3 );
_sfrbit BSY _atbit( ADCON0, 4 );
_sfrbit ADEX    _atbit( ADCON0, 5 );
_sfrbit CLK _atbit( ADCON0, 6 );
_sfrbit BD  _atbit( ADCON0, 7 );

#define bmMX0   0x01
#define bmMX1   0x02
#define bmMX2   0x04
#define bmADM   0x08
#define bmBSY   0x10
#define bmADEX  0x20
#define bmCLK   0x40
#define bmBD    0x80

#define SET_MX0 MX0 = 1;
#define CLR_MX0 MX0 = 0;
#define GET_MX0 MX0
#define SET_MX1 MX1 = 1;
#define CLR_MX1 MX1 = 0;
#define GET_MX1 MX1
#define SET_MX2 MX2 = 1;
#define CLR_MX2 MX2 = 0;
#define GET_MX2 MX2
#define SET_ADM ADM = 1;
#define CLR_ADM ADM = 0;
#define GET_ADM ADM
#define SET_BSY BSY = 1;
#define CLR_BSY BSY = 0;
#define GET_BSY BSY
#define SET_ADEX    ADEX = 1;
#define CLR_ADEX    ADEX = 0;
#define GET_ADEX    ADEX
#define SET_CLK CLK = 1;
#define CLR_CLK CLK = 0;
#define GET_CLK CLK
#define SET_BD  BD = 1;
#define CLR_BD  BD = 0;
#define GET_BD  BD

/* defining bits in SFR ACC */
_sfrbit ACC_0   _atbit( ACC, 0 );
_sfrbit ACC_1   _atbit( ACC, 1 );
_sfrbit ACC_2   _atbit( ACC, 2 );
_sfrbit ACC_3   _atbit( ACC, 3 );
_sfrbit ACC_4   _atbit( ACC, 4 );
_sfrbit ACC_5   _atbit( ACC, 5 );
_sfrbit ACC_6   _atbit( ACC, 6 );
_sfrbit ACC_7   _atbit( ACC, 7 );

#define bmACC_0 0x01
#define bmACC_1 0x02
#define bmACC_2 0x04
#define bmACC_3 0x08
#define bmACC_4 0x10
#define bmACC_5 0x20
#define bmACC_6 0x40
#define bmACC_7 0x80

#define SET_ACC_0   ACC_0 = 1;
#define CLR_ACC_0   ACC_0 = 0;
#define GET_ACC_0   ACC_0
#define SET_ACC_1   ACC_1 = 1;
#define CLR_ACC_1   ACC_1 = 0;
#define GET_ACC_1   ACC_1
#define SET_ACC_2   ACC_2 = 1;
```

```
#define CLR_ACC_2   ACC_2 = 0;
#define GET_ACC_2   ACC_2
#define SET_ACC_3   ACC_3 = 1;
#define CLR_ACC_3   ACC_3 = 0;
#define GET_ACC_3   ACC_3
#define SET_ACC_4   ACC_4 = 1;
#define CLR_ACC_4   ACC_4 = 0;
#define GET_ACC_4   ACC_4
#define SET_ACC_5   ACC_5 = 1;
#define CLR_ACC_5   ACC_5 = 0;
#define GET_ACC_5   ACC_5
#define SET_ACC_6   ACC_6 = 1;
#define CLR_ACC_6   ACC_6 = 0;
#define GET_ACC_6   ACC_6
#define SET_ACC_7   ACC_7 = 1;
#define CLR_ACC_7   ACC_7 = 0;
#define GET_ACC_7   ACC_7

/* defining bits in SFR DIR4 */
_sfrbit P4_0    _atbit( DIR4, 0 );
_sfrbit CM0 _atbit( DIR4, 0 );
_sfrbit P4_1    _atbit( DIR4, 1 );
_sfrbit CM1 _atbit( DIR4, 1 );
_sfrbit P4_2    _atbit( DIR4, 2 );
_sfrbit CM2 _atbit( DIR4, 2 );
_sfrbit P4_3    _atbit( DIR4, 3 );
_sfrbit CM3 _atbit( DIR4, 3 );
_sfrbit P4_4    _atbit( DIR4, 4 );
_sfrbit CM4 _atbit( DIR4, 4 );
_sfrbit P4_5    _atbit( DIR4, 5 );
_sfrbit CM5 _atbit( DIR4, 5 );
_sfrbit P4_6    _atbit( DIR4, 6 );
_sfrbit CM6 _atbit( DIR4, 6 );
_sfrbit P4_7    _atbit( DIR4, 7 );
_sfrbit CM7 _atbit( DIR4, 7 );

#define bmP4_0  0x01
#define bmCM0   0x01
#define bmP4_1  0x02
#define bmCM1   0x02
#define bmP4_2  0x04
#define bmCM2   0x04
#define bmP4_3  0x08
#define bmCM3   0x08
#define bmP4_4  0x10
#define bmCM4   0x10
#define bmP4_5  0x20
#define bmCM5   0x20
#define bmP4_6  0x40
#define bmCM6   0x40
#define bmP4_7  0x80
#define bmCM7   0x80

#define SET_P4_0    P4_0 = 1;
#define CLR_P4_0    P4_0 = 0;
#define GET_P4_0    P4_0
#define SET_CM0 CM0 = 1;
#define CLR_CM0 CM0 = 0;
#define GET_CM0 CM0
#define SET_P4_1    P4_1 = 1;
#define CLR_P4_1    P4_1 = 0;
#define GET_P4_1    P4_1
#define SET_CM1 CM1 = 1;
#define CLR_CM1 CM1 = 0;
#define GET_CM1 CM1
#define SET_P4_2    P4_2 = 1;
#define CLR_P4_2    P4_2 = 0;
#define GET_P4_2    P4_2
#define SET_CM2 CM2 = 1;
#define CLR_CM2 CM2 = 0;
#define GET_CM2 CM2
#define SET_P4_3    P4_3 = 1;
#define CLR_P4_3    P4_3 = 0;
#define GET_P4_3    P4_3
#define SET_CM3 CM3 = 1;
#define CLR_CM3 CM3 = 0;
#define GET_CM3 CM3
#define SET_P4_4    P4_4 = 1;
#define CLR_P4_4    P4_4 = 0;
#define GET_P4_4    P4_4
#define SET_CM4 CM4 = 1;
#define CLR_CM4 CM4 = 0;
#define GET_CM4 CM4
#define SET_P4_5    P4_5 = 1;
#define CLR_P4_5    P4_5 = 0;
#define GET_P4_5    P4_5
#define SET_CM5 CM5 = 1;
#define CLR_CM5 CM5 = 0;
#define GET_CM5 CM5
```

```
895 #define SET_P4_6    P4_6 = 1;
    #define CLR_P4_6    P4_6 = 0;
    #define GET_P4_6    P4_6
    #define SET_CM6 CM6 = 1;
    #define CLR_CM6 CM6 = 0;
900 #define GET_CM6 CM6
    #define SET_P4_7    P4_7 = 1;
    #define CLR_P4_7    P4_7 = 0;
    #define GET_P4_7    P4_7
```